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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/976,490	10/12/2001	Michael C. Dorsey	2070.006400	3412

7590 01/27/2005

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EXAMINER
TRIMMINGS, JOHN P

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 01/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/976,490	DORSEY, MICHAEL C.	
	Examiner	Art Unit	
	John P Trimmings	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/26/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This action is in response to applicant's amendment filed 6/1/2004.

Claims 1-35 are pending in this action.

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 7/26/2004 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Response to Amendment

2. The examiner acknowledges and approves the applicant's changes to the Disclosure, and the examiner withdraws all objections to said Disclosure..

Re: Claim Rejections

3. Applicant's arguments based on the amendment filed 6/1/2004, with respect to the rejection(s)of claim(s) 1-35 under 35 USC § 112(2), 102(b), and 103(a) have been fully considered and are persuasive. Therefore, the rejections have been withdrawn. However, upon further consideration, a new grounds of rejection is made in view of the addition of the following limitation to the independent claims: "wherein the dual-mode built-in self-test controller is geographically centralized within an integrated circuit".

Claim Rejections - 35 USC § 103

4. Claims 1, 2, 4, 6, 9-15, 19, 21-23 and 31-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Au et al., U.S. Patent No. 6681359, in view of Motika et al., U.S. Patent No. 6000048, and further in view of Kohno, U.S. Patent No. 5943285.

As per Claim 1:

Au et al. teaches a BIST controller (see FIG.3 MBIST CONTROL 116) comprising a 2nd frequency domain in which memory self-test is performed (FIG.3 BIST_CLK 110) and a 3rd frequency domain used for test interface (FIG.3 TAP CONTROLLER 112 and TCK 106). However, Au et al. does not teach a 1st frequency domain for a logic test circuit, but in an analogous art, Motika et al. teaches differing frequency domains (column 2 lines 50-65) used for ABIST and for LBIST (logic circuit) testing (see FIG.2 frequency generator 26 which feeds circuits 30). And, wherein the generator is being used for the advantage of improving thermal stress in test (column 1 lines 60-64), one with ordinary skill in the art at the time of the invention, motivated as suggested by Motika, would combine the two references. But, not taught by Au et al. and Motika et al. is wherein the dual-mode built-in self-test controller is geographically centralized within an integrated circuit. But in an analogous art, Kohno does teach this feature (see Abstract, and column 8 lines 8-27. And in column 1 lines 6-9 and column 5 lines 57-67, the inventor cites advantages of less restricted design requirements while maintaining fast circuit speed. One with ordinary skill in the art at the time of the invention, motivated as suggested, would find it obvious to apply the centralized theme

of Kohno to the controller taught by Au et al. and Motika et al. in order to produce a better self-testing product.

As per Claim 2:

Dependent on Claim 1, the claim limits the 1st clock signal (logic) is derived from the 3rd clock signal (test interface). In Motika et al., FIG.2, both of the logic and memory clock signals are derived from a reference clock (FIG.2 "REF CLK") from the outside test source (column 3 lines 22-39) such as a tester interface. And in view of the motivation previously stated for Motika et al., one with ordinary skill in the art at the time of the invention would combine the references for this claim, and so it is rejected.

As per Claim 4:

Dependent on Claim 1, limits clocks 1, 2 and 3 to 150, 75, and 10 MHz respectively. The claims of reference, in specifying the clocks and their usage, does not require that the frequencies be of any specific number. Therefore, one with ordinary skill in the art at the time of the invention, would interpret the references as to be all encompassing in terms of clock frequency, and so would include the frequencies stated in the applicant's claim. And in view of the motivation previously stated for Claim 1, this claim is rejected.

As per Claim 6:

The claim limits Claim 1 further wherein the memory test generates a plurality of step clock signals. These clock signals are the equivalent of BIST_CLK 110 in Au et al., FIG.3, and under control of the TAP CONTROLLER 112, the clocks continue to run until

the test terminates with the TEST_DONE BIT in FIG.5 182. And in view of the motivation previously stated for Claim 1, this claim is rejected.

As per Claim 9:

The claim is dependent on Claim 1, and limits the 2nd clock domain to being a memory self-test engine (Au et al., FIG.3 MBIST CONTROL 116) that executes the self-test (Au et al., column 8 lines 13-55). And in view of the motivation previously stated for Claim 1, the claim is rejected.

As per Claim 10:

The hardware of Claim 9 above is further limited to a self-test signature register for storing test results. Au et al., in column 8 lines 13-55 describes the MBIST testing wherein the test results are stored in scan register cells 114 for eventual scanning through the TAP interface. And in view of the motivation previously stated for Claim 9, the claim is rejected.

As per Claim 11:

The hardware of Claim 9 above is further limited to a MBIST self-test state machine (Au et al., FIG.3 MBIST CONTROL 116, and column 9 lines 25-33, and a nested BIST engine (FIG.3 TAP CONTROLLER 112, and column 9 lines 7-24) operating the respective state machine. And in view of the motivation previously stated for Claim 9, the claim is rejected.

As per Claim 12:

The hardware of Claim 9 above is further limited to plural MBIST self-test state machines (Au et al., FIG.3 MBIST CONTROL 116 – there are 4 in the example), and

the self-test engine (FIG.3 TAP CONTROLLER 112) operating one of the state machines (Au et al. column 3 lines 54-62) and therefore testing one memory circuit. And in view of the motivation previously stated for Claim 9, the claim is rejected.

As per Claim 13 and 21:

Au et al. teaches a BIST controller (see FIG.3 MBIST CONTROL 116) and a JTAG test interface (Au et al. see Abstract), comprising a 2nd frequency domain in which memory self-test is performed (FIG.3 BIST_CLK 110) and a 3rd frequency domain used for test interface (FIG.3 TAP CONTROLLER 112 and TCK 106). Also taught by Au et al. is a plurality of memory components (FIG.3 136 - there are 4). However, Au et al. does not teach a 1st frequency domain for a logic core, but in an analogous art, Motika et al. teaches differing frequency domains (column 2 lines 50-65) used for ABIST and for LBIST (logic core) testing (see FIG.2 frequency generator 26 which feeds circuits 30). And, wherein the generator is being used for the advantage of improving thermal stress in test (column 1 lines 60-64), one with ordinary skill in the art at the time of the invention, motivated as suggested by Motika, would combine the two references, and so the claims are rejected. But, not taught by Au et al. and Motika et al. is wherein the dual-mode built-in self-test controller is geographically centralized within an integrated circuit. But in an analogous art, Kohno does teach this feature (see Abstract, and column 8 lines 8-27. And in column 1 lines 6-9 and column 5 lines 57-67, the inventor cites advantages of less restricted design requirements while maintaining fast circuit speed. One with ordinary skill in the art at the time of the invention, motivated as suggested,

would find it obvious to apply the centralized theme of Kohno to the controller taught by Au et al. and Motika et al. in order to produce a better self-testing product.

As per Claim 14:

Dependent on Claim 13, the claim limits the 1st clock signal (logic) is derived from the 3rd clock signal (test interface). In Motika et al., FIG.2, both of the logic and memory clock signals are derived from a reference clock (FIG.2 "REF CLK") from the outside test source (column 3 lines 22-39) such as a tester interface. And in view of the motivation previously stated for Motika et al., one with ordinary skill in the art at the time of the invention would combine the references for this claim, and so it is rejected.

As per Claim 15:

Dependent on Claim 13, limits clocks 1, 2 and 3 to 150, 75, and 10 MHz respectively. The claims of reference, in specifying the clocks and their usage, does not require that the frequencies be of any specific number. Therefore, one with ordinary skill in the art at the time of the invention, would interpret the references as to be all encompassing in terms of clock frequency, and so would include the frequencies stated in the applicant's claim. And in view of the motivation previously stated for Claim 13, this claim is rejected.

As per Claim 19:

The claim is dependent on Claim 13, and limits the 2nd clock domain to being a memory self-test engine (Au et al., FIG.3 MBIST CONTROL 116) that executes the self-test (Au et al., column 8 lines 13-55). And in view of the motivation previously stated for Claim 13, the claim is rejected.

As per Claim 22:

The claim is to a method for use in performing a built-in self-test, the method comprising receiving an external clock signal in a testing interface (Motika et al., FIG.2 "REF CLK"), the external clock signal defining a first frequency domain (F1G.2 PLL 24), generating a first internal clock signal (FIG.2 OPCG output to LBIST), the first internal clock signal defining a second frequency domain in which a logic built-in self-test may be performed (FIG.2 LBISTI; and generating a second internal clock signal (FIG.2 OPCG output to ABIST), the second internal clock signal defining a third frequency domain in which memory built-in self-test may be perïormed (FIG.2 ABIST). But, not taught by Motika et al. is wherein the dual-mode built-in self-test controller is geographically centralized within an integrated circuit. But in an analogous art, Kohno does teach this feature (see Abstract, and column 8 lines 8-27. And in column 1 lines 6-9 and column 5 lines 57-67, the inventor cites advantages of less restricted design requirements while maintaining fast circuit speed. One with ordinary skill in the art at the time of the invention, motivated as suggested, would find it obvious to apply the centralized theme of Kohno to the controller taught by Au et al. and Motika et al. in order to produce a better self-testing product.

As per Claim 23:

The method of claim 22, wherein generating the first internal clock signal (Motika et al. FIG.2 OPCG output to LBIST) includes generating the first internal clock signal from the external clock signal (Motika et al., FIG.2 "REF CLK"). And in view of the motivation previously stated, the claim is rejected.

As per Claim 31:

The claim describes a method for testing an integrated circuit device, and Au et al. teaches a method comprising: interfacing the integrated circuit device with a tester (Au et al., column 1 lines 18-33 and column 3 lines 8-20); performing a built-in self-test (column 3 lines 1-7), including: receiving an external clock signal in a testing interface from the tester (FIG.3 TCK 106), the external clock signal defining a first frequency domain (TAP CONTROLLER); generating a first internal clock signal (FIG.3 TEST_H 126), and obtaining the results of the built-in self-test (Au et al., column 3 lines 1-7). However, Au et al. does not specifically describe how clock signals are derived. But Motika et al., in an analogous art teaches this in that the first internal clock signal (Motika et al. FIG.2 105 defines a second frequency domain (FIG.2 output of OPCG 26) in which a logic built-in self-test may be performed (FIG.2 LBIST 34); and generating a second internal clock signal (FIG.2 other output of OPCG 26), the second internal clock signal defining a third frequency domain in which memory built-in self-test may be performed (FIG.2 ABIST 32). And in view of the previous motivation for Motika et al., the claim is rejected. But, not taught by Au et al. and Motika et al. is wherein the dual-mode built-in self-test controller is geographically centralized within an integrated circuit. But in an analogous art, Kohno does teach this feature (see Abstract, and column 8 lines 8-27. And in column 1 lines 6-9 and column 5 lines 57-67, the inventor cites advantages of less restricted design requirements while maintaining fast circuit speed. One with ordinary skill in the art at the time of the invention, motivated as suggested, would find it

obvious to apply the centralized theme of Kohno to the controller taught by Au et al. and Motika et al. in order to produce a better self-testing product.

As per Claim 32:

Taught by Au et al in FIG.3. in addition to the teachings of Claim 31 is, wherein generating the first internal clock signal (FIG.3 TEST_H 126) includes generating the first internal clock signal from the external clock signal (FIG.3 TCK 106). And in view of the above motivation, the claim is rejected.

As per Claim 33:

Dependent on Claim 31, limits clocks 1, 2 and 3 to 150, 75, and 75 MHz respectively. The claims of reference, in specifying the clocks and their usage, does not require that the frequencies be of any specific number. Therefore, one with ordinary skill in the art at the time of the invention, would interpret the references as to be all encompassing in terms of clock frequency, and so would include the frequencies stated in the applicant's claim. And in view of the motivation previously stated for Claim 31, this claim is rejected.

As per Claim 34:

The method of claim 31, wherein performing the built-in self-test includes performing a logic built-in self-test is also taught by Motika et al. (FIG.2 LBIST 34), and in view of the motivation above, the claim is rejected.

5. Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Au et al., U.S. Patent No. 6681359, and in view of Motika et al., U.S. Patent No. 6000048 and Kohno, U.S. Patent No. 5943285 as applied to Claim 13 above, and in

view of Arimilli et al., U.S. Patent No. 6665828, and further in view of "Reducing Test Data Volume using External/LBIST Hybrid Test Patters", Das et al., ITC Test Conference 2000, October 3-5, 2000, pp 115-122.

As per Claim 16:

The controller of Claim 13 is limited as follows: the LBIST internal test of the circuit described by Arimilli et al. (FIG.3) encompasses a loading process (LSSD clocking as per the subject claim) whereby the test data is scanned into the circuit under test (FIG.6 606 and 603), but the application of test patterns by a step clock is not specifically described even though a PRPG is used. And in this reference, the inventor cites improved testing with less internal wiring (column 2 lines 2-6) in LSSD testing. One with ordinary skill in the art at the time of the invention, motivated by Arimilli et al., would combine the references, and so the claim is rejected.

As per Claim 17:

Claim 13 is further limited in that the LBIST circuit described by Das et al. describes what occurs after data is loaded (page 116 column 1 paragraph 4, step 1) into a PRPG, wherein the LBIST test pattern is run a fixed number of times (step clocking as per the subject claim). And Das et al. cites improved testing coverage with a Hybrid approach (see Abstract of paper, page 115). One with ordinary skill in the art at the time of the invention, motivated by Das et al., would combine the references, and so the claim is rejected.

6. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Au et al., U.S. Patent No. 6681359, and in view of Motika et al., U.S. Patent No. 6000048 and

Kohno, U.S. Patent No. 5943285, as applied to Claim 13 above, and in view of Koproski et al., U.S. Patent No. 6671838. The claims limit the logic circuit of Claim 13 to comprising an LBIST engine for executing tests and storing results in a MISR. Koproski et al., in FIG.1 illustrates an LBIST with a state machine (LBIST engine/state machine, column 2 lines 60-67 and column 3 lines 1-5), and result storage (FIG.1 MISR 12). Koproski et al., in column 2 lines 5-28 describes the advantage to be a better, flexible and custom approach to random pattern generation. One with ordinary skill in the art at the time of the invention would combine the references to attain this result, and in view of the motivation attributed to Koproski et al., the claim is rejected.

7. Claims 3 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Au et al., U.S. Patent No. 6681359, and in view of Motika et al., U.S. Patent No. 6000048 and Kohno, U.S. Patent No. 5943285, as applied to Claims 2 and 13 above, and further in view of Krishna et al., U.S. Patent No. 6000048.

As per Claim 3:

The claim, dependent on Claim 2, limits the clocks in that the 2nd clock (memory) is derived from the 1st clock (test interface). Krishna et al., in FIG.2, shows the base clock (CLK 34) feeding the frequency generator 36 that is in turn passing on the multiplied clock frequency through the logic circuit 54 to the memory 32. Therefore, the clock in the memory is derived from the logic circuit. In column 3 lines 28-42, Krishna et al. states an advantage of being able to test large memories using a VLSI tester. And one with ordinary skill in the art at the time of the invention, motivated by Krishna et al., would combine the references, and so the claim is rejected.

As per Claim 20:

The claim, dependent on Claim 13, limits the memory to an SRAM. Krishna et al., in FIG.2 teaches the inclusion of an SRAM in the makeup of the device, and in view of the motivation for Krishna et al previously stated, the claim is rejected.

8. Claims 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Motika et al., U.S. Patent No. 6000048 and Kohno, U.S. Patent No. 5943285, as applied to Claim 22 above, and further in view of Krishna et al., U.S. Patent No. 6000048. The claims, dependent on Claim 22, limit the clocks in that the 2nd clock (memory) is derived from the 1st clock (test interface). Krishna et al., in FIG.2, shows the base clock (CLK 34) feeding the frequency generator 36 that is in turn passing on the multiplied clock frequency through the logic circuit 54 to the memory 32. Therefore, the clock in the memory is derived from the logic circuit. In column 3 lines 28-42, Krishna et al. states an advantage of being able to test large memories using a VLSI tester. Also, the claims of reference, in specifying the clocks and their usage, does not require that the frequencies be of any specific number. Therefore, one with ordinary skill in the art at the time of the invention, would interpret the references as to be all encompassing in terms of clock frequency, and so would include the frequencies stated in the applicant's claim 25. And in view of the motivation previously stated for Krishna et al., the claims are rejected.

9. Claims 26-29 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Motika et al., U.S. Patent No. 6000048 and Kohno, U.S. Patent No. 5943285, as applied to Claim 22 above, and further in view of Krishna et al., U.S. Patent No.

6000048. These claims of method are being interpreted by the examiner as being in the same frequency domains as claimed by the applicant for the device. Based on the art referenced, these claims bear similarity to the device claims in the following manner; Claim 26 = Claims 16 & 17; Claims 27 & 28 = Claim 18 and Claim 35; and Claim 29 = Claim 19. Based on the rejection of the device claims, the subject method claims are similarly rejected.

10. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Motika et al., U.S. Patent No. 6000048 and Kohno, U.S. Patent No. 5943285, as applied to Claim 22 above, and further in view of Lo et al., U.S. Patent No. 5661732. The claim limits the MBIST to include resetting a memory built-in self-test engine (Lo et al. column 6 lines 31-37); initiating a plurality of components and signals in the third frequency domain upon receipt of a memory built-in self-test run signal (column 5 lines 5-20); flushing the contents of a plurality of memory components to a known state (column 13 lines 6-10) after initialization of the components and the signals; and testing the flushed memory components (column 13 lines 5-20). Lo et al., in column 2 lines 1-31 lists the advantages of this invention, among the advantages is to reduce BIST redesign. One with ordinary skill in the art at the time of the invention, motivated by Lo et al. as suggested, would combine the references, and so the claim is rejected.

11. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Au et al., U.S. Patent No. 6681359, in view of Motika et al., U.S. Patent No. 6000048, and further in view of Kohno, U.S. Patent No. 5943285 as applied to Claim 1 above, and in view of Arimilli et al., U.S. Patent No. 6665828, and further in view of "Reducing Test Data

Volume using External/LBIST Hybrid Test Patters", Das et al., ITC Test Conference 2000, October 3-5, 2000, pp 115-122. The controller of Claim 1 is limited as follows: the LBIST internal test of the circuit described by Arimilli et al. (FIG.3) encompasses a loading process (LSSD clocking as per the subject claim) whereby the test data is scanned into the circuit under test (FIG.6 606 and 603), but the application of test patterns by a step clock is not specifically described even though a PRPG is used. And in this reference, the inventor cites improved testing with less internal wiring (column 2 lines 2-6) in LSSD testing. The subject claim is further limited in that the LBIST circuit described by Das et al. describes what occurs after data is loaded (page 116 column 1 paragraph 4, step 1) into a PRPG, wherein the LBIST test pattern is run a fixed number of times (step clocking as per the subject claim). And Das et al. cites improved testing coverage with a Hybrid approach (see Abstract of paper, page 115). One with ordinary skill in the art at the time of the invention, motivated by both Arimilli et al. and Das et al., would combine the references, and so the claim is rejected.

12. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Au et al., U.S. Patent No. 6681359, in view of Motika et al., U.S. Patent No. 6000048, and further in view of Kohno, U.S. Patent No. 5943285 as applied to Claim 1 above, and in view of Koproski et al., U.S. Patent No. 6671838. The claims limit the logic circuit of Claim 1 to comprising an LBIST engine for executing tests and storing results in a MISR, and with a pattern generator powering the application of signals. Koproski et al., in FIG.1 illustrates an LBIST with a state machine (LBIST engine/state machine, column 2 lines 60-67 and column 3 lines 1-5), and result storage (FIG.1 MISR 12), with signals

applied through a random pattern generator (FIG.1 2). Koproski et al., in column 2 lines 5-28 describes the advantage to be a better, flexible and custom approach to random pattern generation. One with ordinary skill in the art at the time of the invention would combine the references to attain this result, and in view of the motivation attributed to Koproski et al., the claim is rejected.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P Trimmings whose telephone number is 571-272-

3830. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John P Trimmings
Examiner
Art Unit 2133

jpt

Guy J. Lamarre
Primary Examiner